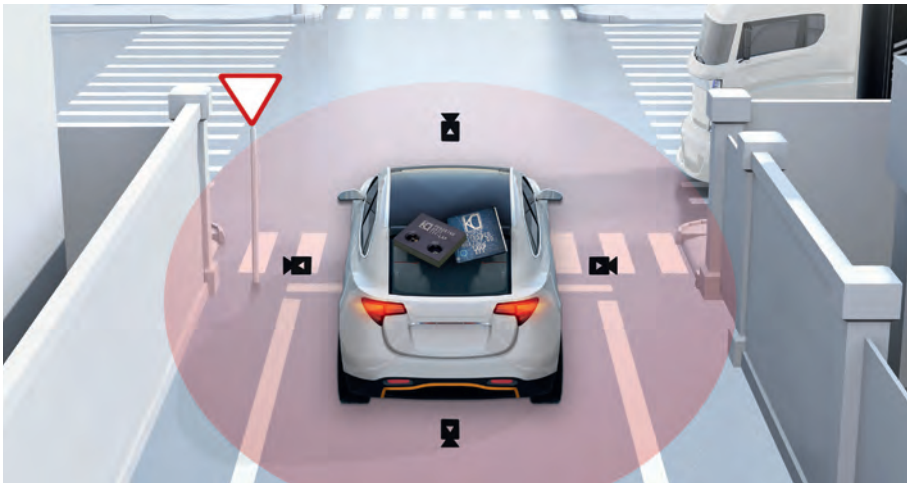
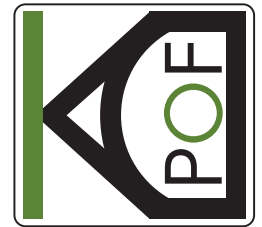


Optical High-speed Connectivity

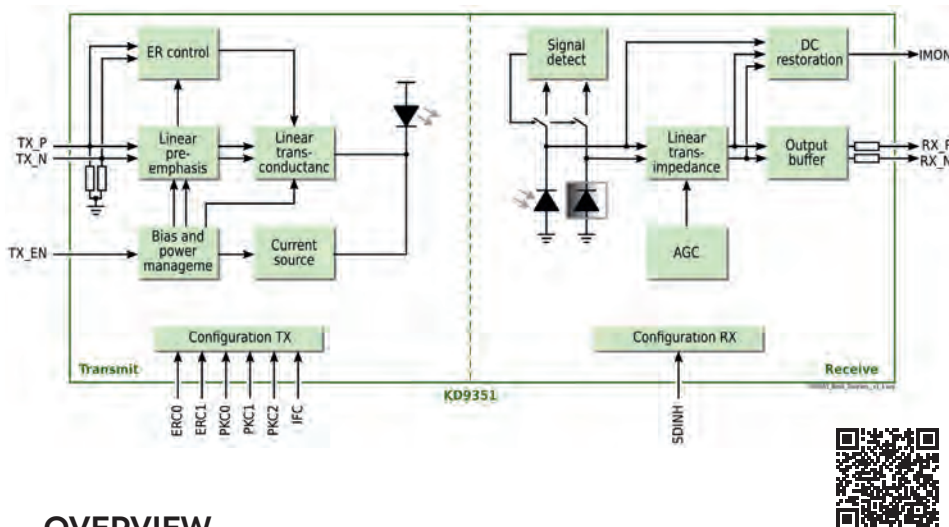


The KD9351 integrated Fiber Optic Transceiver (FOT) complements the KD1053 IC, providing competitive pricing for EMC critical or galvanic isolated critical links in automotive networks. Optimized for low power, reduced BOM and a small footprint, the KD1053 and KD9351 devices are targeted for automotive applications that use optical Ethernet over Plastic Optical Fiber (POF) for the communications in vehicle data networks. Interconnection of infotainment and Advanced Driver Assistance Systems (ADAS) ECUs are two of the key applications where POF is the best choice.

FEATURES

- 1 Gb/s operation mode, 1000BASE-RHC Physical Medium Dependent (PMD) sublayer according to the IEEE Std 802.3bv™-2017
- 100 Mb/s operation for applications requesting low data rates and high optical link margin
- Optimized for multimode plastic optical fiber with the channel characteristics specified by IEEE Std 802.3bv™-2017 Clause 115
- Wake-up & Sleep support as per ISO 21111
- Guaranteed BER < 10^{-12} for 1 Gb/s and 100 Mb/s operation modes, when operating with KD1053 PCS-PMA transceiver
- Single 3.3 V supply
- Low power consumption (see below)
- Low-cost bill of materials (BOM)
- Integrated EMC shielding, compliant with CISPR25 Class-5 at component level
- Automotive AEC-Q100 grade 2
- -40 to +105 °C operating ambient temperature
- 36-pin LGA (7 x 8 mm) package

KD9351 – Automotive 1000BASE-RHC PMD Integrated Transceiver



OVERVIEW

The KD9351 is a Fiber Optic Transceiver that implements the Physical Medium Dependent Sublayer (PMD) of a 1000BASE-RHC PHY, compliant with the specifications of IEEE Std 802.3bv™-2017 standard for gigabit optical communications over POF. The KD9351 connects with the KDPOF KD1053 transceiver, which implements a Physical-Coding Sublayer (PCS) and a Physical Medium Attachment (PMA) sublayer, to form a complete automotive 1000BASE-RHC physical layer. With its integrated EMC shielding, the KD9351 transceiver guarantees the highest component-level EMC compliance without the need for any external additions. It can operate either at 1 Gb/s or 100 Mb/s.

TRANSMITTER SIDE

- High and controlled Extinction-Ratio (ER) for link budget maximization: 15 dB (typ.)
- Linear pre-emphasis circuitry for LED acceleration
- Designed to be connected to a differential, current steering DAC, with two interface possibilities (typical values):
 - DAC full-scale current 6 mA, DAC source single ended termination 50 Ω
- Current consumption (normal operation mode, typ. value): 74.9 mA

RECEIVER SIDE

- Integrated trans-impedance amplifier (TIA) and differential photo-diode
- DC restoration
- Automatic gain control (AGC) to guarantee a constant voltage amplitude regardless of the received photo-current
- Signal-detection signaling
- Current consumption (normal operation mode, typ. value): 37.3 mA

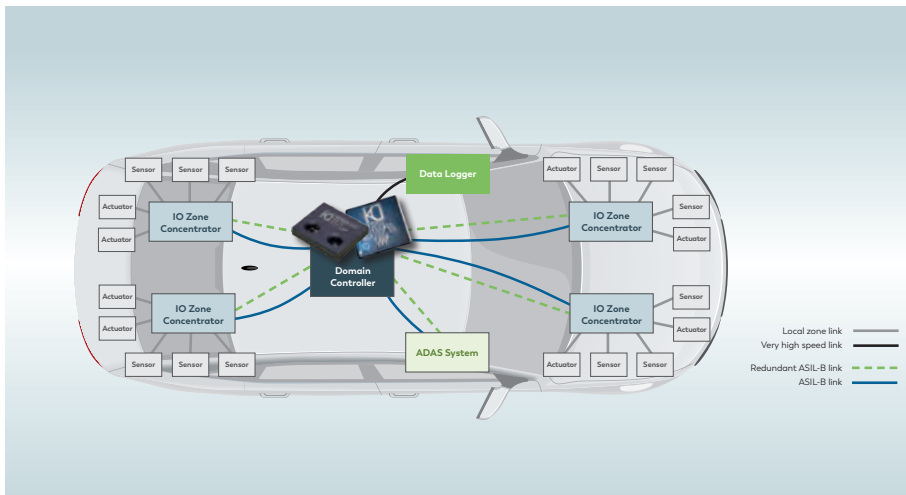


KDPOF
pr@kdpof.com
Tel: +34 918043387

© KDPOF. Specifications can be changed without notice.

www.kdpof.com

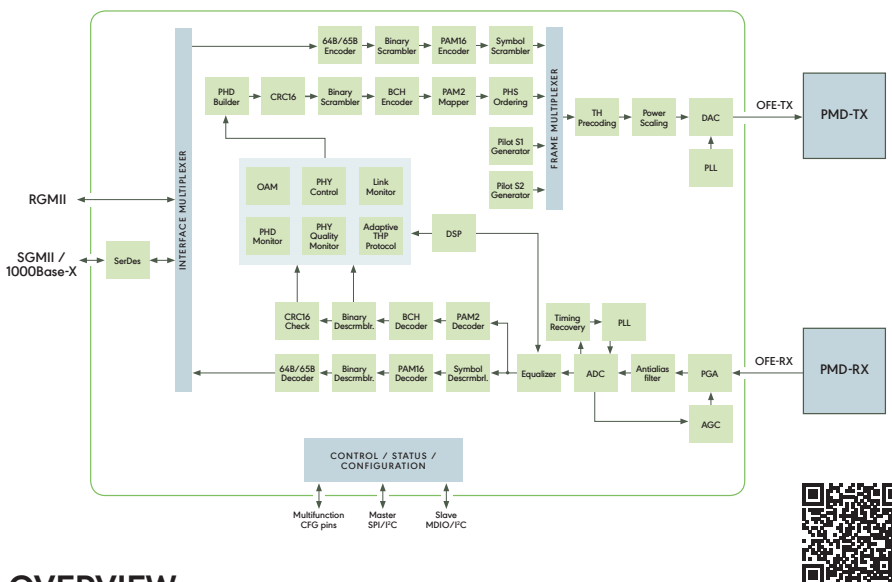
Optical High-speed Connectivity



FEATURES

- In 1 Gb/s operation mode, 1000BASE-H Physical Coding Sub-layer (PCS) and the Physical Medium Attachment (PMA) sublayers according to the IEEE Std 802.3bv™-2017
- 100 Mb/s operation mode supported for applications requesting low data rates and high optical link margin
- Specified for multimode plastic optical fiber with the channel characteristics specified by IEEE Std 802.3bv™-2017 Clause 115. Designed to operate:
 - at 1 Gb/s with the fiber optic channel type II and type III according to Clause 115 of IEEE Std 802.3bv™-2017;
 - at 100 Mb/s with 120 m of SI-POF without in-line connectors, or with 40 m with up to 10 in-line connectors
- Support RGMII v2.0, RMII, MII, SGMII, 1000BASE-X and 100BASE-X standards in the MAC interface
- Support 1.8V 2.5V and 3.3V LVTTTL digital I/O standard for parallel MAC interface; and 2.5V LVDS for serial MAC interface
- SMI (MDC/MDIO) interface for configuration and monitoring supporting Clauses 22 and 45, which can be configured as an I²C bus
- SPI/I²C master interface for reading external boot and configuration EEPROM memory
- Support for IEEE, OAM, Wake-up & Sleep, interruption generation
- Support for jumbo packets up to 10 KB
- PTP and Sync-E supported
- Different loopback modes and PMD test-modes for diagnostics
- Link/activity monitoring and speed LED outputs
- Support for high-level ASIL systems
- Fully integrated digital adaptive non-linear equalizers
- BER < 10⁻¹² for 1 Gb/s and 100 Mb/s operation modes
- 6.2 us latency for 1 Gb/s operation and 1.4 us for 100 Mb/s (local RGMII to remote RGMII); 5 ns RMS jitter for 1 Gb/s operation and 9 ns for 100 Mb/s
- 55 ms of link time for 1 Gb/s operation
- Internal dependability functions: power supply, process and temperature sensors; and FOT received power monitoring
- Advanced power management with integrated linear voltage regulators for 2.5V: it can be supplied with only external 1.2V and 3.3V power voltages
- Low power, 460 mW at 1 Gb/s
- Low-cost bill of materials (BOM)
- Designed to be EMC compliant with CISPR25 Class-5 at component level
- 65 nm CMOS process
- Automotive AEC-Q100 grade 2
- -40 to +105 °C ambient temperature range
- 56-pin QFN (7 x 7 mm) ROHS package

KD1053 – Automotive 1000BASE-H Transceiver



OVERVIEW

The KD1053 is a 65 nm CMOS ASIC that implements the Physical-Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer of a 1000BASE-RHx PHY, compliant with the specifications of IEEE Std 802.3bv™-2017 standard for gigabit optical communications over Plastic Optical Fiber (POF). The KD1053 must be connected to a compatible Fiber Optics Transceiver (FOT), which implements a Physical Medium Dependent (PMD) sublayer and a Medium Dependent Interface (MDI), to form a complete automotive 1000BASE-RHC physical layer. The KD1053 implements the following optional features of IEEE Std 802.3bv™-2017: 1000BASE-H Operations Administration Maintenance (OAM) channel, support for Energy Efficient Ethernet (EEE) mode, exposed Management Data Input/Output (MDIO), and motor vehicle environmental requirements.

The KD1053 can operate at 100 Mb/s and 1 Gb/s. It is optimized for EMC compatibility, low power, reduced BOM, and a small footprint. Its built-in analog interface simplifies connectivity to the Physical Medium Dependent (PMD) sublayer. It supports different parallel and serial MAC interfaces for connecting a MAC station, an MCU or a switch. The KD1053 transceiver provides a Serial Management Interface (SMI), also called an MDC/MDIO interface, and a master SPI/I²C port to access an external EEPROM memory for configuration. The transceivers' parallel MAC interface pins are 1.8V, 2.5V and 3.3V LVTTTL compliant; and serial MAC interfaces are 2.5V LVDS.



KDPOF
pr@kdpof.com
Tel: +34 918043387

© KDPOF. Specifications can be changed without notice.

www.kdpof.com