Towards the Multi-Gigabit Ethernet for the Automotive Industry

A. Rodríguez-Pérez, R. Pérez de Aranda, E. Prefasi, J. San Pablo, S. Dumont, , J. Rosado, I. Enrique, P. Pinzón and D. Ortiz

***Abstract*—This paper shows the status of the Ethernet-based communication solutions, focused on optical links, for the automotive industry. First, the implementation of a product compatible with the 1000BASE-RHC according to the IEEE Std 802.3bv is presented, which is the first able to transmit 1Gbps over POF for automotive. Second, a new architecture to achieve up to 25Gbps for automotive is described. The proposed Multi-Gigabit system leverages existing technologies, as VCSELs, multi-mode fibers and photodiodes already developed for the data centers industry.**

Keywords—High-speed optical communication, TIA, high-speed ADC, VCSEL driver, LED driver, Ethernet transceiver.

I. Introduction

Until now, the automotive market has relied on low-speed networks, like Controlled Area Network (CAN) or Local Interconnect Network (LIN), in order to connect the remote sensors to the Electronic Control Units (ECUs). For higher speed links, such as infotainment, Media-Oriented System Transport (MOST) was used, where the speed is limited to 150 Mbps. However, all these links have started to be insufficient to cover the future automotive market needs. Advancements in the infotainment and the evolution towards the autonomous vehicle through the Advanced Driver-Assistance Systems (ADAS) are imposing a huge increase in the real-time data shared by the ECUs. The automotive industry foreseen that for the close future, speeds up to 25Gbps for the In-Vehicle Network (IVN), will be needed.

Ethernet is one of the most extended standards for communication systems in both commercial and industrial applications. One of its key attributes is the capability of sending data between two nodes of the same network over many different routes. This capability eases the introduction of redundancy and the ability to define a wide range of network topologies, which is critical to the functionality and reliability of the future IVNs.

Automotive industry imposes stringent requirements: extreme operating conditions (-40ºC to +105ºC ambient temperature), high reliability, low cost, stringent Electro-Magnetic Compatibility (EMC) requirements, and Bit Error Rate (BER) below 10^{-12}. Therefore, the industry was forced to develop specific Ethernet standards for the automotive applications. This is the case of the standardized IEEE 802.3 PHY types 100BASE-T1 and 1000BASE-T1 for links over balanced twisted-pair cables.

However, one of the main problems of the electrical links is that they are prone to emit electromagnetic noise and are highly susceptible to electromagnetic noise, so their implementation in some sections of the cars usually generates big problems to the Original Equipment Manufacturers (OEMs). Also, the proliferation of electric cars has imposed the need of providing a galvanic isolation among the high voltage batteries domain and the low voltage electronics. An alternative is to use optical links, which do not suffer from these drawbacks. To this end, another standard, IEEE Std 802.3bv, which defines PHY type 1000BASE-RHC for 1Gbps transmission over Plastic Optical Fiber (POF) for automotive applications, was developed in IEEE. Also, other study group has started to develop the future Multi-Gigabit Automotive Optical Ethernet PHYs.

In this work we show two different solutions for optical based communications. Section II shows a full system for 1Gbps, which has been already fabricated and qualified according to the automotive standards. In section III the main circuits and components for a Multi-Gigabit system are discussed. Some conclusions are derived in section IV.

II. Gigabit Ethernet over Pof

The IEEE standard amendment for 1000Mb/s Ethernet operation over POF, IEEE Std 802.3bv (also called GEPOF), defines the physical layer specifications and management parameters for automotive, industrial, and home networking applications utilizing Step-Index POF (SI-POF) [1]. This standard sets the starting point for the development of Ethernet optical communications for the automotive industry. The motivation of this standard was to re-use as much as possible the medium (1mm diameter POF fibre), Light Emitting Diode (LED), Si PIN diode, and connectors that were used in MOST [2], exploiting the Shannon capacity of the channel to deliver 1Gbps with high link budget. In order to compensate the low bandwidth of the leveraged components, the signal is modulated in amplitude using PAM16 with a symbol rate of 325MBd.

Fig. 1 shows the implementation of the two components that compose a GEPOF port. One component is called PHY controller, implementing the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sub-layer of the standard, and another one is called Fibre Optical Transceiver (FOT), which embeds the Physical Medium Dependent (PMD) sub-layer and the Medium Dependent Interface (MDI).

A. PHY controller

The block diagram of the PHY controller is shown in Fig. 2. The PCS transmit function encodes Ethernet frames coming from the Gigabit Media Independent Interface (GMII) input into 65-bits blocks (i.e. 64b/65B encoding) and then scrambles it. Afterwards, the data is encoded and mapped using a Multi-Level Coset Code (MLCC) block-oriented encoder, which generates fixed-length code-words of PAM16 symbols, which are further scrambled. MLCC codewords are encapsulated using a series of Transmit Blocks, which also includes pilot signals and control

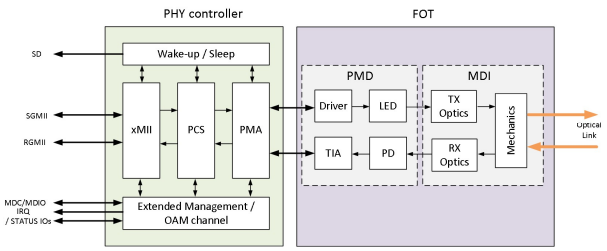

Fig. 1: Two component implementation of the GEPOF system

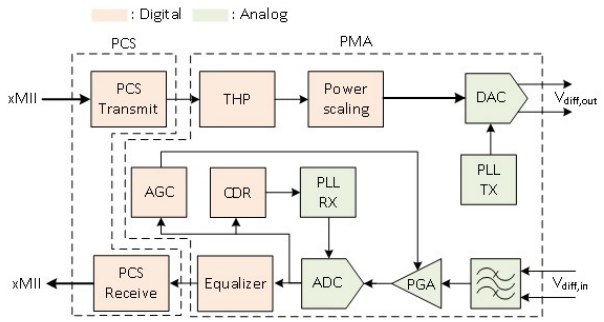

Fig. 2: Block diagram of PHY controller

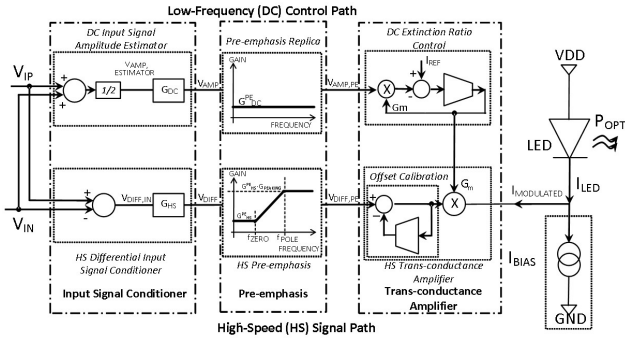

Fig. 3: Schematic of the LED driver

information to allow the remote receiver being aligned. The PAM16 symbols are then transferred to the PMA transmit function, which comprises the Tomlinson-Harashima Precoding (THP), able to pre-compensate the post-cursor part of the Inter-Symbol Interference (ISI) produced in the communication channel due to the limited bandwidth [3][4]. The power scaling produces similar dynamic range in every part of the Transmit Block before the symbols are transmitted to the PMD sublayer. Then the digital data is transferred to a 9-bit, 325MS/s current-steering Digital-to-Analog Converter (DAC), which generates a differential signal for the LED driver in the FOT device.

The receiver is also shown in Fig. 2. The differential input signal ($V_{diff,in}$) coming from the Trans-Impedance Amplifier (TIA) passes through a 162.5MHz anti-alias filter, based on a Nauta's transconductor topology optimized to save area and power [5]. After the filter, a Programmable Gain Amplifier (PGA) is introduced to maximize the voltage swing to the input of the ADC. The converter is implemented as a 10-bit 325MS/s pipeline architecture and generates the stream for the digital processor. The Clock Data Recovery (CDR) adjusts the control bits of a fractional-N PLL in order to generate the optimum sampling clock for the ADC. The CDR includes coarse timing recovery for symbol synchronization and fine timing recovery. This way, a stable clock to sample the received signal from the PMD is provided with a suitable phase for reliable reception. Equalization is performed using the adaptive THP protocol coordinated between the receiver and link partner transmitter [1]. The receiver estimates the coefficients to be used in the local filters and the ones of the THP to be used by the remote PHY transmitter, based on the pilots of the received frame. Due to the fact that the harmonic distortion of the LED (specially the 2nd order coefficients) is very high, the PMA receiver implements additionally non-linear channel response. The linearization filters are local to the receiver and does not coordinate with the remote transmitter.

B. FOT component

The FOT component embeds the photonics (photodiode and LED), the associated optoelectronics (TIA and LED driver), and the optics and mechanics to align the fibre and focus the light.

Fig. 3 shows the schematic of the LED driver [6]. It receives the differential input voltage from the DAC. Then, it generates an output current to drive the LED. The LED emits the modulated output light as a function of the received input signal that is transmitted through the POF. The LED driver shows a high linear response (more than 40dB) in order to accommodate the resolution needed to transmit the PAM16 signal. Moreover, the LED driver implements a pre-emphasis filter in order to enhance the high frequency LED response, which is limited to a bandwidth of around 70MHz. The output average current (i.e. LED bias current) sets the Average Optical Power (AOP) of the transmitted light, and is determined by a fixed current source coming from an internal current conveyor. The modulated input signal, after going through the pre-emphasis filter, is then transformed into current by means of a high speed transconductor. The output current is then summed up to the bias current to generate the modulated output current injected to the LED. The driver also includes a low frequency path to calibrate the equivalent transconductance applied to the input signal as function of the input differential voltage level. This ensures that the Extinction Ratio (ER) of the transmitted optical signal is always under control, independently of the DAC and the driver input process variations.

Fig. 4 shows the schematic of the TIA [7]. This block receives the photocurrent generated by the photodiode exposed to the incident light. Then, the TIA multiplies the photocurrent by a given transimpedance and produces an output differential voltage that is transmitted to the PMA of the PHY controller. It uses a fully differential topology in order to improve the Common-Mode Rejection Ratio (CMRR) and Power-Supply Rejection Ratio (PSRR). For doing it, the photodiode is also differential and is formed by two PIN diodes, one exposed and one covered. The TIA implements a feedback topology, which is optimum in terms of noise [8]. In order to improve the linearity of the TIA response, the feedback resistance R_f is built by means of a set of parallel nMOS transistors in linear region with

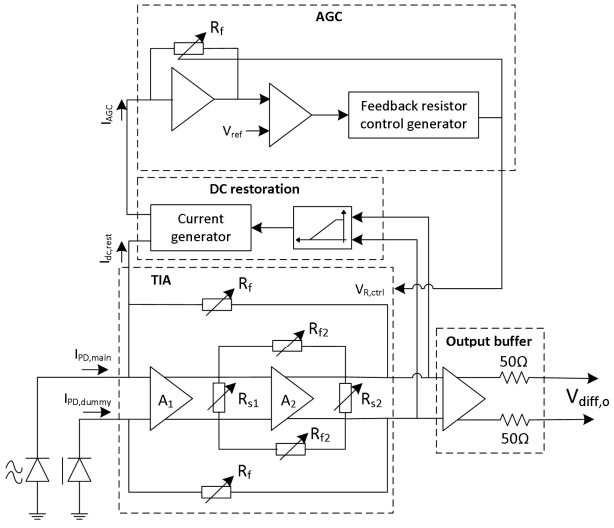

Fig. 4: Schematic of the TIA

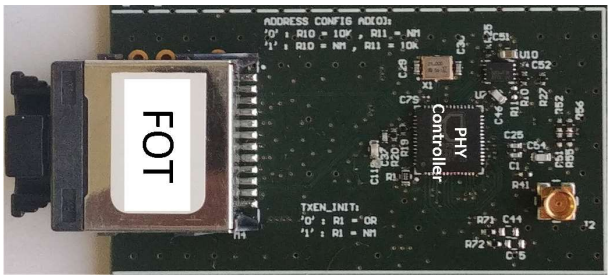

Fig. 5: Photography of the GEPOF system PCB

programmable gate voltage. The DC component of the incident light is removed by means of the DC restoration block. Since this DC component represents the input AOP, it is used to control the applied transimpedance by means of the Automatic Gain Control (AGC) block. The AGC embeds a copy of the main TIA topology and uses an integral closed-loop to set the control voltage of the transimpedance resistors. In order to guarantee the stability of the core amplifier when reducing the feedback resistance, the TIA also includes some programmable resistors (R_{s1}, R_{f2} and R_{s2}) to control the equivalent gain of the core amplifier. The TIA response gives a good linearity (above 40dB) over the complete transimpedance range (from 600Ω up to 300kΩ). The TIA is the main noise source of the system. In order to establish the link without errors the input referred noise of the TIA is minimized. The output of the TIA is buffered to be connected to the anti-alias filter of the PMA in the PHY controller.

Fig. 5 shows photography of both the PHY controller and FOT components in the PCB, forming a port compatible with the GEPOF standard. Both components have been fully qualified according to AEC-Q100 Grade 2. The system is able to set a successful 1Gbps link on 15m POF cable using up to 4 inline connectors. The performance has been tested for an ambient temperature range of -40ºC to +105ºC and an operating life of more than 15 years.

III. Multi-Gigabit Optical Ethernet PHY

The Multi-Gigabit Optical Ethernet PHY presented in this section follows the same technology leveraging approach than the one presented in section II. This means that it is based on exploiting as much as possible the limits of the mature photonics and optical channels, which are used in other markets and standards, taking advantage of scale economy. In one hand, Vertical Cavity Surface Emitting Lasers (VCSELs) and GaAs photodiodes are selected as they are extensively used in the industry. In the other hand, optical fibres with huge scale economy, such as Multi-Mode Fibers (MMF) OM3 (50 um grade-index core), are used.

Traditionally, optical systems are composed by two separated components, as illustrated in Fig. 1: one embedding the optics, photonics and optoelectronics (FOT), and another one with the main digital processing (PHY controller). The main advantage of this approach is that the optics can be encapsulated within a small chip. Also, the optoelectronics can be fabricated in a special process, such as BiCMOS, SiGe and Heterojunction Bipolar Transistor (HTB), to optimize its design. However, the main drawback is that the two components are physically separated in the PCB layout (see Fig. 5), imposing stringent constraints in the design of the interconnection of the two blocks, and becoming a critical path regarding electromagnetic compatibility.

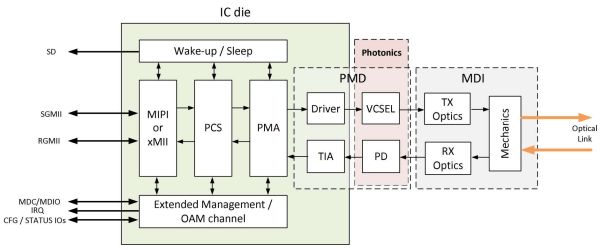

Fig. 6: Single component implementation of the Multi-Giga optical Ethernet system

In order to override these problems, we propose a single CMOS chip approach, like the one shown in Fig. 6, where both the PCS and PMA are implemented with the optoelectronics. This chip is integrated in a common substrate to the external photonics, and attached to the optics which, together with the mechanics will be connected to the fibre. This solution has the following advantages:

- Simplifies the PCB design
- Reduces the cost of the final solution, since the port is built by one single component.
- Saves power consumption because it removes the high-speed interfaces between the FOT and the PHY.
- Solve the EMI/EMS and signal integrity problems of the electrical interfaces between separate components, especially critical in Multi-Gigabit data-rates.

A. Transmitter

Due to its low-cost and ease of integration, VCSELs have been largely used for short-range optical data communication applications during the last decades [9]. Its reliability is highly dependent on the temperature and current density, so the only way to ensure its lifetime is to reduce the current density as the operating temperature increases [10]. The current density reduction impacts on the VCSEL performance, reducing its bandwidth and emitted optical power, and increasing its Relative Intensity Noise (RIN). Furthermore, the VCSEL process variation is big. Oxide aperture diameter can vary in a range of ±60%, which greatly impacts on the current threshold and the achievable reliability. Due to that, it is necessary to implement an adaptive driver that allows high yield and reduced cost.

In order to optimize the design of the VCSEL driver, a model based on the extraction of the DC and AC parameters of the VCSEL has been built [11]. To this end, several InGaAs VCSEL samples with different oxide apertures have been measured using a Vector Network Analyzer (VNA) for

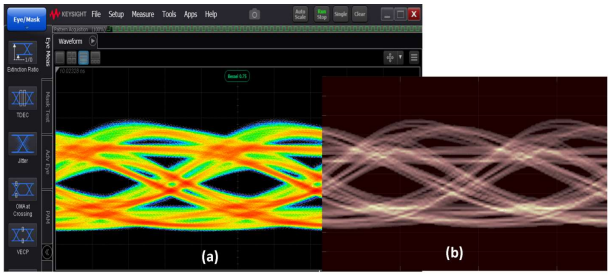

Fig. 7: Verification of the VCSEL model: (a) measured eye-diagram, (b) simulated eye-diagram

different bias currents (1mA to 10mA) and substrate temperatures (from -40ºC to 125ºC). The model has been verified against real transient large signal measurements, as Fig. 7 shows, and can be considered trustworthy to carry out time-domain communication system simulations, to obtain receiver sensitivity and make link budget assessment.

B. Receiver

The receiver is formed by a feedback TIA, followed by a Variable Gain Amplifier (VGA) and a 5-bit, 26.5GS/s Time-Interleaving ADC (TI-ADC). This architecture allows a very good scalability in speed by means of adjusting the number of channels in the TI-ADC. The digital processor embeds, together with the digital equalization and the CDR, a DSP-oriented on-line calibration to compensate clock skew, gain and bandwidth mismatches and offsets of the TI-ADC.

As the TIA is the main noise source of the system, it has been modelled taking into account the technological parameter levels of a sub-nanometric CMOS technology in order to optimize its design and do the system-level simulations.

C. Technology comparison

IEEE Std 802.3 10GBASE-SR and 25GBASE-SR specifications are considered as starting point to develop the Multi-Gigabit optical PHY for automotive applications. However, they present important gaps for these applications as they are not designed to the automotive operating conditions and the lifetime requirements. To solve these issues, the proposed technology includes the support for DSP-based advanced timing recovery and channel equalization together with a low complexity FEC. This allows reaching a sensitivity improvement through impairment compensation, when compared to the mentioned standards. Adaptive electronics are used to compensate Process, Voltage and Temperature (PVT) variations and to allow the use of low current densities VCSEL driving, making possible to reach reliability criteria of automotive industry.

The proposed communication system has been designed to support speeds between 2.5Gbps and 25Gbps using 850nm VCSEL single lane. The different speeds share a unique physical layer scheme (same FEC, encoding, etc.), while the symbol rate is scaled accordingly. The technology feasibility is demonstrated by simulation considering the following factors:

- Automotive extreme environmental conditions.
- High reliable link (BER < 10^{-12})
- Worst case channel insertion loss conditions extracted from real optical connectivity implementations designed for harsh environments.
- Extreme parametric deviations in critical components (VCSEL, photodiode, CMOS).
- Reliability imposed limitations.

The system model was built taking into account the models described in the transmitter and receiver sub-sections and compared against already standardized solutions, i.e. 10GBASE-SR and 25GBASE-SR, assuming that all of them would use the same photonics, optics, electrical implementation technology node and environmental constraints. The comparison is shown in Table 1 in terms of link budget and margin. Only solutions with positive link margin are feasible.

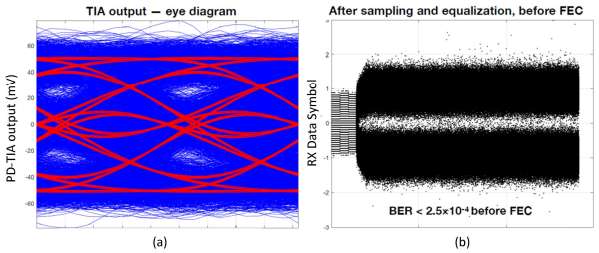

Fig. 8: Transient performance of the proposed Multi-Gigabit systems in the sensitivity point: (a) Eye diagram of the TIA output, (b) Received data symbol after sampling and equalization, before FEC

Table 1: Sensitivity comparison for nGBase-SR and the proposed nGiga system

	10Gb/s Base-SR	**25Gb/s Base-SR**	**10Gb/s proposal**	**25Gb/s proposal**
OMA_{PD} (dBm)	-12.82	-10.46	-21.18	-15.97
OMA_{TP3} (dBm)	-10.82	-8.46	-19.18	-13.97
Link budget (dB)	3.82	1.46	12.18	6.97
Link Margin (dB)	-0.98	-3.34	7.38	2.17

In order to illustrate the capacity of the proposed system, Fig. 8(a) shows the eye diagram at the receiver in the sensitivity point (i.e., the minimum input power that guarantees a reliable link). It can be observed that, due to the Inter-Symbolic Interference (ISI) and the noise of the system, the eye is completely closed, and no symbol can be distinguished. Even after equalizing this input data, the Signal-to-Noise (SNR) of the input data stream is too low to ensure a BER below 10^{-12}, as illustrated Fig. 8(b). This figure shows an initial stage where both the CDR and equalizers are converging. Once the internal loops have converged, the main data distribution is clearly visible, but the high noise of the system makes a lot of received symbols to fall into an uncertainty area that increases the BER of the system before the FEC decoder. Then, FEC decoding allows improving the BER to the desired levels below 10^{-12}.

IV. Conclusions

This paper has presented solutions to enable optical-based communications for the automotive industry. One is the implementation of a product that is able to set a 1Gbps link over SI-POF, based on the IEEE Std 802.3bv. The presented work is a fully qualified product according to AEC-Q100 Grade 2. The other one is a novel architecture proposal of an optical transceiver able to transmit up to 25Gbps. The proposed system is able to exploit the maximum capacity of existing mature components, such as VCSELs, multi-mode fibers and photodiodes already developed for the data-centers industry. The proposed solution leverages this technology to make it work for automotive industry. This is achieved by means of DSP-based advanced timing recovery and channel equalization, low complexity FEC and adaptive electronics to compensate PVT. The advantage of the proposed system is demonstrated by comparison with the current 10GBASE-SR and 25 GBASE-SR standards.

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